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L9: Entry 14 of 18 File: USPT Jul 4, 2000

US-PAT-NO: 6085208
DOCUMENT-IDENTIFIER: US 6085208 A

TITLE: Leading one prediction unit for normalizing close path subtraction results within a floating point arithmetic unit

DATE-ISSUED: July 4, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Oberman; Stuart F.	Sunnyvale	CA		
Roberts; Mark	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 09/ 049758 [PALM]
DATE FILED: March 27, 1998

INT-CL: [07] G06 F 5/00

US-CL-ISSUED: 708/205; 708/211
US-CL-CURRENT: 708/205; 708/211

FIELD-OF-SEARCH: 708/205, 708/211

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4922446	May 1990	Zurawski et al.	708/205
☐	5369607	November 1994	Okamoto	708/505
☐	5867407	February 1999	Wolrich et al.	708/205
☐	5920493	July 1999	Lau	708/205
☐	5957997	September 1999	Olson et al.	708/205

OTHER PUBLICATIONS

E. Hokenek and R. K. Montoye, "Leading-zero anticipator in the IBM RS/6000 floating-point execution unit," IBM Journal of Research and Development, vol. 34, No. 1, pp. 71-77, Jan. 1990.
N. T. Quach and M. J. Flynn, "Leading one prediction--Implementation,

generalization, and application," Technical Report No. CSL-TR-91-463, Computer Systems Laboratory, Stanford University, Mar. 1991.

ART-UNIT: 277

PRIMARY-EXAMINER: Malzahn; David H.

ATTY-AGENT-FIRM: Conley, Rose & Tayon, PC Kivlin; B. Noel Christen; Dan R.

ABSTRACT:

An optimized multimedia execution unit configured to perform vectored floating point and integer instructions. In one embodiment, the execution unit includes an add/subtract pipeline having far and close data paths. The far data path is configured to handle effective addition operations, as well as effective subtraction operations for operands having an absolute exponent difference greater than one. The close data path, conversely, is configured to handle effective subtraction operations for operands having an absolute exponent difference less than or equal to one. The execution unit may also include a plurality of add/subtract pipelines, allowing vectored add, subtract, and integer/floating point conversion instructions to be performed. The execution unit may also be expanded to handle additional arithmetic instructions (such as reverse subtract and accumulate functions) by appropriate input multiplexing. The execution unit may also be configured with a leading one prediction unit that is configured to predict the position of a leading one value for certain results in order to improve normalization times.

41 Claims, 88 Drawing figures

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L9: Entry 16 of 18 File: USPT Mar 30, 1999

US-PAT-NO: 5889984
DOCUMENT-IDENTIFIER: US 5889984 A
** See image for Certificate of Correction **

TITLE: Floating point and integer condition compatibility for conditional branches and conditional moves

DATE-ISSUED: March 30, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mills; Jack D.	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 699424 [PALM]
DATE FILED: August 19, 1996

INT-CL: [06] G06 F 9/00

US-CL-ISSUED: 395/566; 395/563
US-CL-CURRENT: 712/225; 712/222

FIELD-OF-SEARCH: 395/566, 395/567, 395/568, 395/564, 395/563, 395/800.41

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5367705	November 1994	Sites et al.	395/564
☐	5410682	April 1995	Sites et al.	395/564
☐	5469551	November 1995	Sites et al.	395/800.41
☐	5568624	October 1996	Sites et al.	395/564
☐	5685009	November 1997	Blomgren et al.	395/566

OTHER PUBLICATIONS

Sites et al., Alpha Architecture Reference Manual, pp. 1.4-1.6, 3.1-3.2,4.28, 4.78-4.79, 4.92-4.93,4.98-4.99, Jun. 1992.
MC88110, Second Generation RISC Microprocessor User's Manual, pp. 10-35,10-44, 10-56, Dec. 1991.

ART-UNIT: 278

PRIMARY-EXAMINER: Ellis; Richard L.

ASSISTANT-EXAMINER: Winder; Patrice L.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman LLP

ABSTRACT:

In a processor where separate integer and floating point units are utilized, conditions generated in the integer unit are transferred and made compatible for use in the floating point unit by floating point conditional branch and move operations. Conversely, conditions generated in the floating point unit are transferred and made compatible for use in the integer unit by integer conditional branch and move operations. By providing semantic compatibility of conditions with conditional operations in both integer and floating point units, conditions can be generated in one numeric unit and operated in the other.

14 Claims, 9 Drawing figures

L9: Entry 16 of 18 File: USPT Mar 30, 1999

DOCUMENT-IDENTIFIER: US 5889984 A
** See image for Certificate of Correction **
TITLE: Floating point and integer condition compatibility for conditional branches and conditional moves

Detailed Description Text (19):
Referring to FIG. 6, it depicts the flow of data for specified instructions in the case of a condition that is generated in the integer register file. In FIG. 6 (as well as in the subsequent FIG. 7) oval shapes represent instructions, rectangles represent registers, and arrows are used to indicate the flow of data as a result of the instructions. An integer compare instruction (CMP) 30 is defined to write either all ones or all zeroes into its destination register 13a depending on whether its two sources bear the specified relationship (equal to, less than, greater than, etc.) to each other. An integer conditional move instruction (CMOV) 31 is defined to read all bits of its condition source register (which will be register 13a) and copy its second or third source into its destination depending on the value of the condition of the source register 13a. An integer conditional jump instruction (CJMP) 32 is defined to read one or more, or all bits in its condition source register 13a and branch (or not branch) as a function of this value. Thus, the integer compare operation communicates to the integer conditional jump and conditional move operations via bit value(s) in a specified integer register 13a.

Detailed Description Text (23):
Referring to FIG. 7, it depicts the flow of data for the case of a condition that is generated in the floating point register file. A floating point compare instruction (FCMP) 40 is defined to write either all ones or all zeroes into its destination register 23b depending on whether its two sources bear the specified relationship to each other. The floating point conditional move instruction (FCMOV) 41 is employed to read the sign bit of its condition source register 23b and copy its second or third source into its destination depending on the value of the condition in source register 23b. The floating point conditional jump instruction (FCJMP) 42 is employed to read the sign bit of its condition source register 23b and branch (or not branch) as a function of this value. Thus, the floating point compare operation communicates to the floating point conditional jump and conditional move operations via the sign bit in a floating point register 23b.

First Hit Fwd Refs

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L4: Entry 7 of 9 File: USPT Apr 1, 2003

US-PAT-NO: 6542990
DOCUMENT-IDENTIFIER: US 6542990 B1

TITLE: Array access boundary check by executing BNDCHK instruction with comparison specifiers

DATE-ISSUED: April 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tremblay; Marc	Menlo Park	CA		
O'Connor; James Michael	Union City	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Santa Clara	CA			02

APPL-NO: 10/ 118388 [PALM]
DATE FILED: April 8, 2002

PARENT-CASE:
CROSS-REFERENCE SECTION This application is a continuation of U.S. patent application Ser. No. 09/565,625, filed May 4, 2000, and entitled, "Array Access Boundary Check By Executing BNDCHK Instruction With Comparison Specifiers," and naming Marc Tremblay and James Michael O'Connor as the inventors, now issued U.S. Pat. No. 6,408,383, the application being incorporated herein by reference in its entirety.

INT-CL: [07] G06 F 12/06

US-CL-ISSUED: 712/227; 711/152, 711/171, 712/208, 712/225
US-CL-CURRENT: 712/227; 711/152, 711/171, 712/208, 712/225

FIELD-OF-SEARCH: 711/152, 711/171, 712/225, 712/227, 712/208

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4760374	July 1988	Moller	340/146.2
☐	5568624	October 1996	Sites et al.	712/223